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\* \*PCI EXPRESS is considered to be the most general purpose bus so it should appeal to a wide audience in this arena. \*Today's buses are becoming more specialized to meet the needs of the particular system applications, building the need for this book.

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architecture utilizes PCI to PCI (P2P) bridges to extend the number of devices that can be supported on the bus. By definition a system built from P2P bridges forms a

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### **PCI Express (PCIe) Overview - Flash Memory Summit**

These free resources are available to the Intel® Developer Network for PCI\* Express Architecture community. PCI Express\* Specifications. The PHY Interface for the PCI Express\* (PIPE) Architecture Revision 5.1.1 is an updated version of the PIPE spec that supports PCI Express\*, SATA, USB, DisplayPort, and Converged I/O architectures.

### **PCI Express\* Architecture - Intel**

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### **PCI Express Basics & Background**

The various system components are described along with the services they provide. This paper will also define common terms used when describing Intel architecture designs and their operation.

### **Introduction to Intel® Architecture**

7/23 PCI and PCI Express Bus Architecture Computer Science & Engineering Department Arizona State University Tempe, AZ 85287 Dr. Yann-Hang Lee yhlee@asu.edu

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